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THE FUTURE OF CHIP-TO-WAFER STACKING TECHNOLOGIES

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Séverine CHERAMY _ Leti Workshop @ Semicon West | July 10, 2018

3D IC MARKET DRIVERS

PERFORMANCE

COST

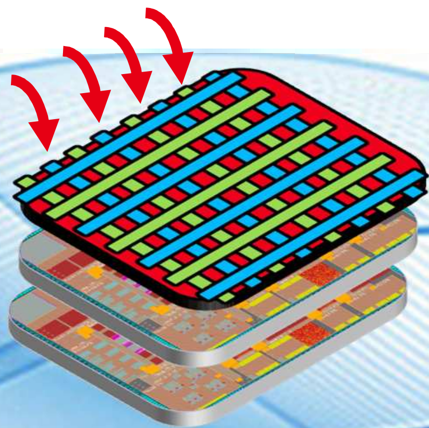
FORM FACTOR

Adapted from Yole Business Report

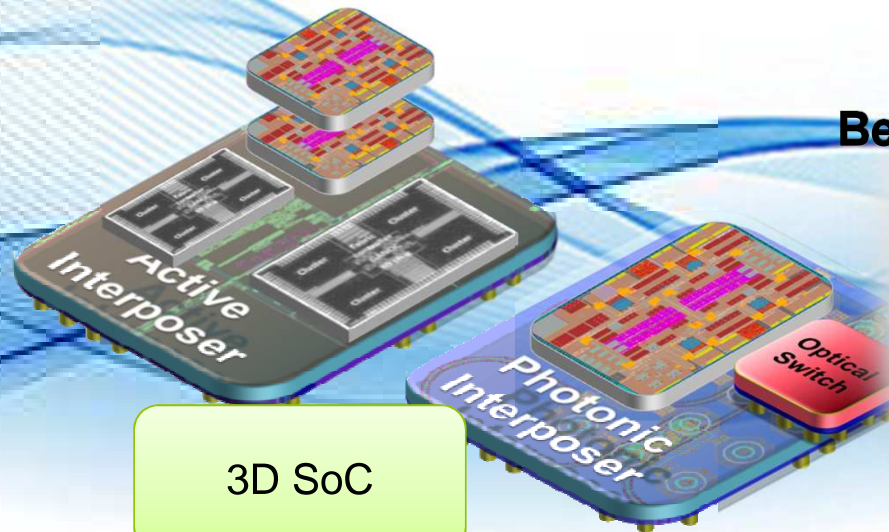
BUILDING 3D VLSI FOR NEXT WAVE OF INNOVATION

- Scalability
- Dedicated die function
- IP re-use
- Compact
- Performances

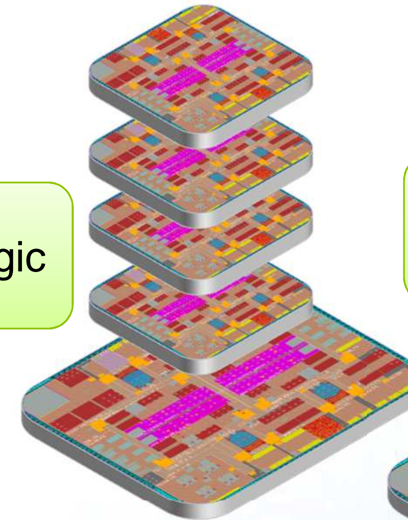
- ….And cost!



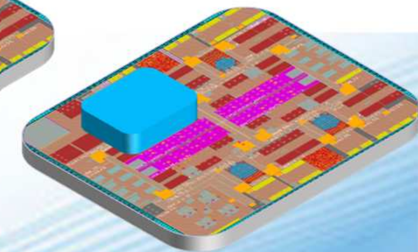
Sensor / Logic + Memory



3D SoC



SRAMs / Logic

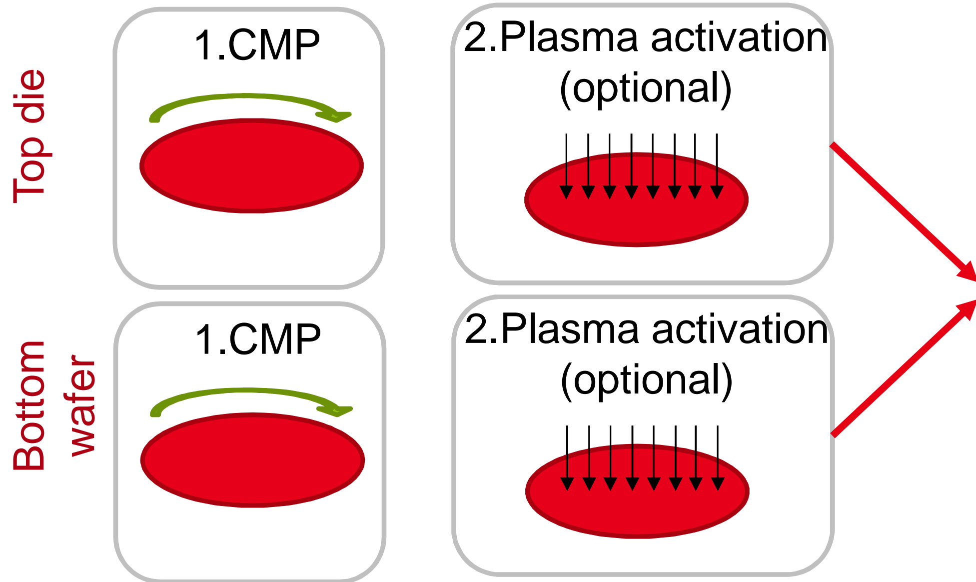


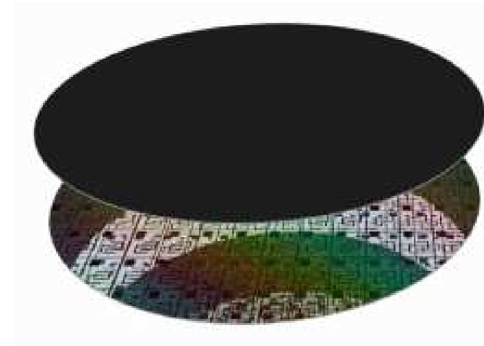
Non-CMOS Componant / Logic

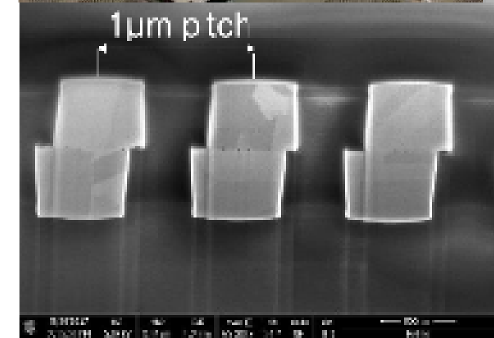
Benefits of Direct-Hybrid Bonding

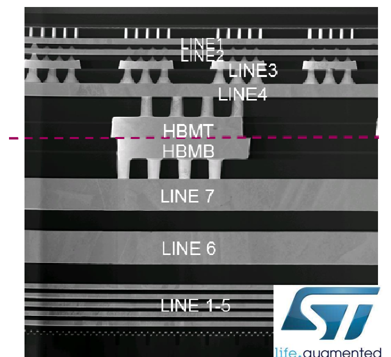
Very fine pitch
Less Underfill
High performance (incl @ HF)
High reliability

FROM WAFER-TO-WAFER DIRECT HYBRID BONDING FLOW …



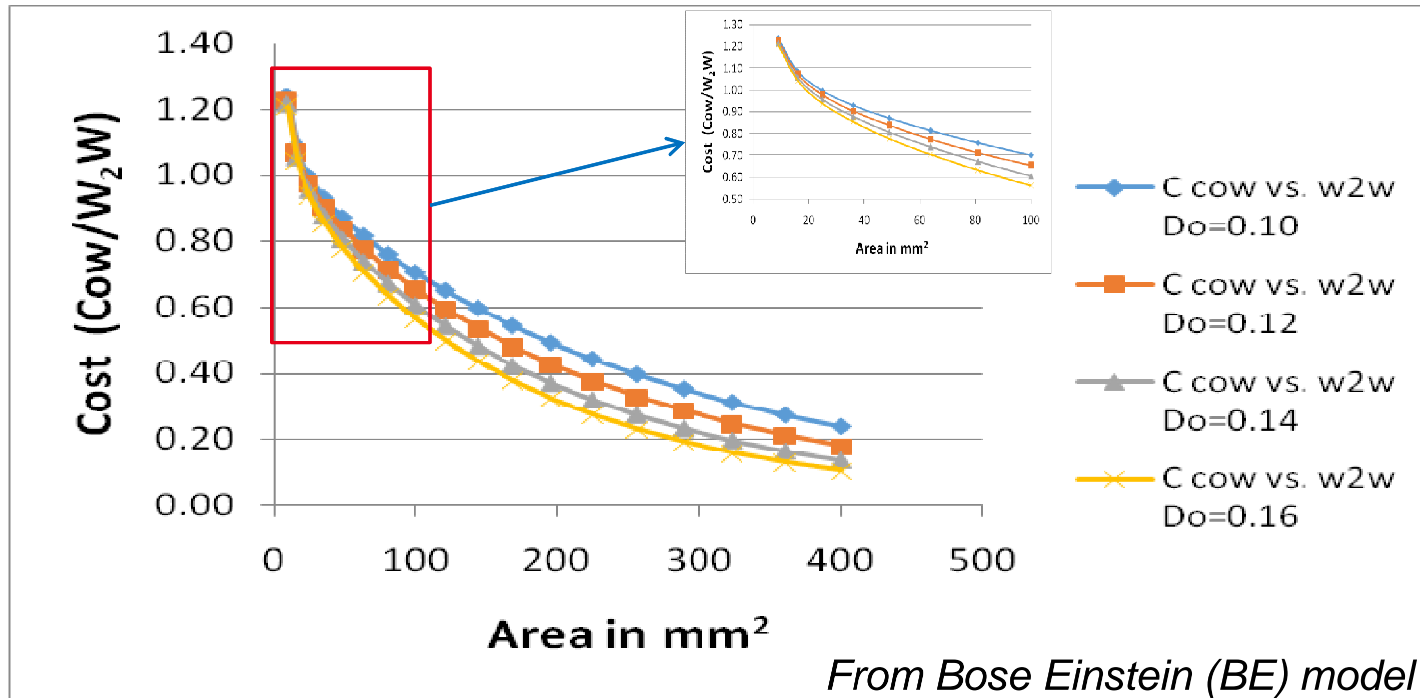






Take advantage of wafer-to-wafer expertise

RELEVANCE OF WAFER-TO-WAFER VS DIE-TO-WAFER COST POINT OF VIEW



S3S 2017, D. Gitlin & Al, Generalized Cost Model for 3D Systems

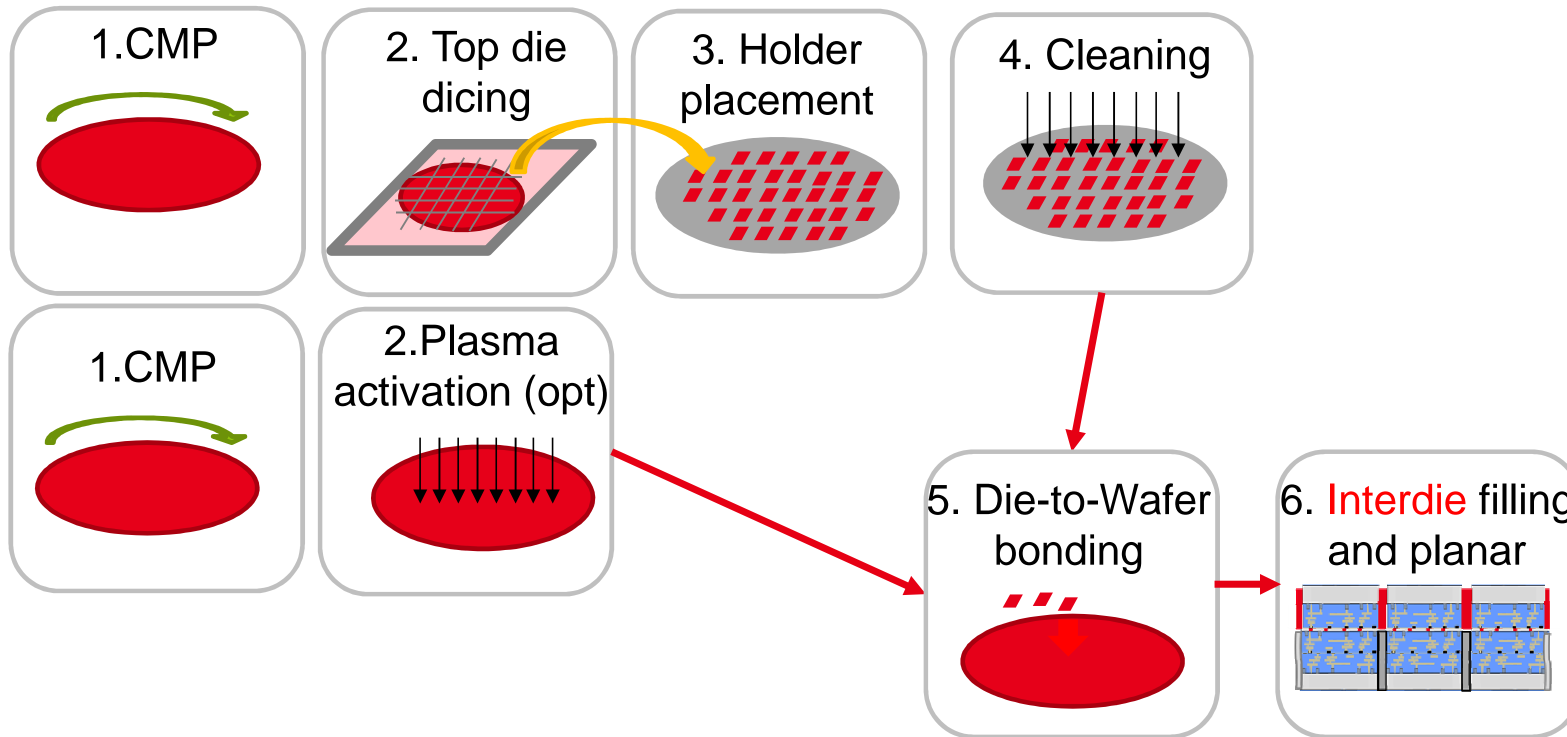
Key message

Except for small dies, **DtW is more cost effective than W2W** approach from an architecture point of view…

….Performances are more or less similar (pitch, RLC, delay…)

….Processes maturity is similar

....TO DIE-TO-WAFER HYBRID BONDING FLOW

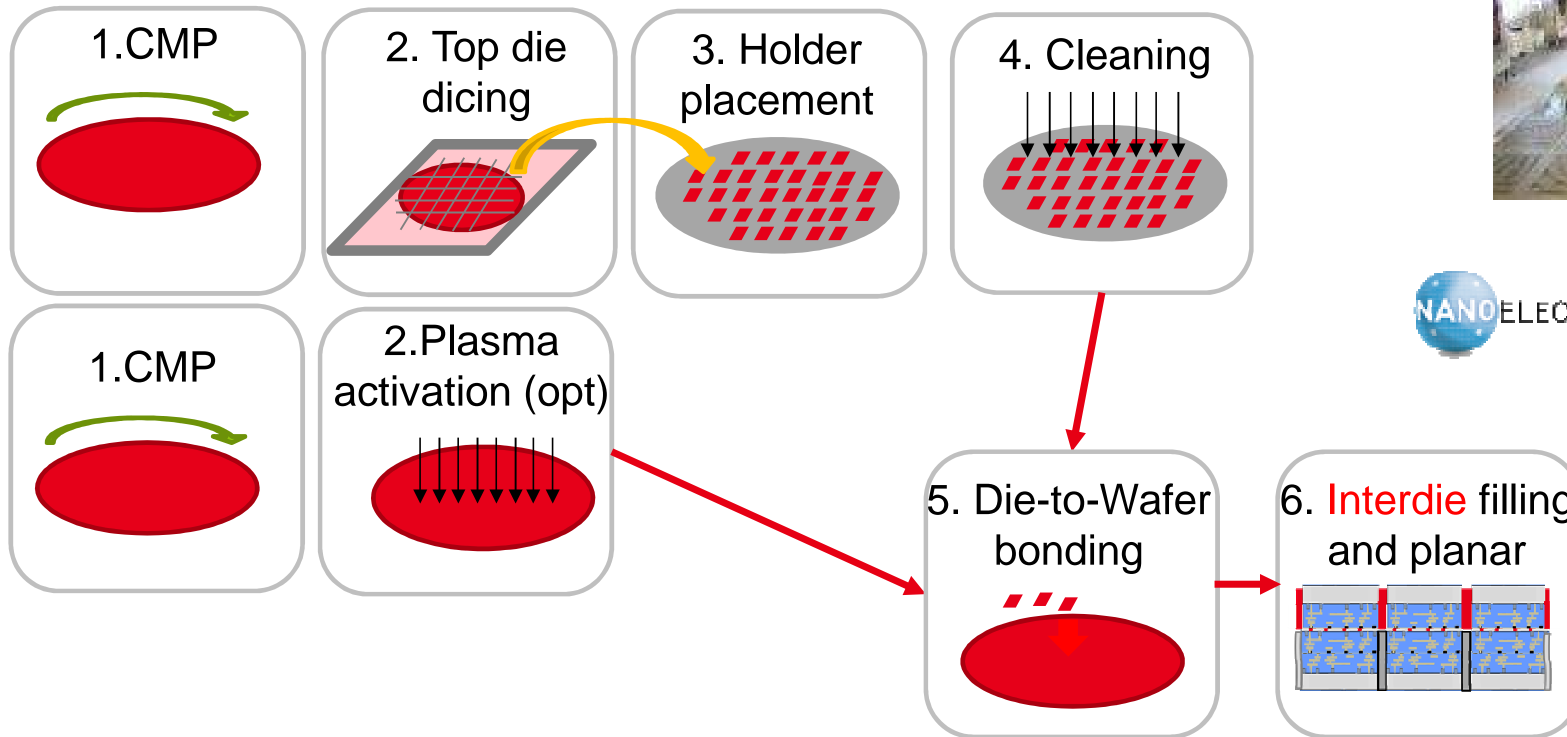


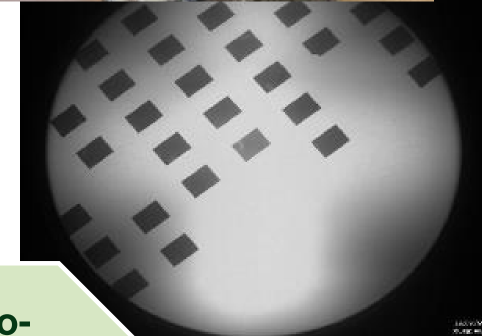
Requirements for the Die-Bonder

- Atmosphere in the tool: **no particle contamination**
- **Die handling:** no contact with the active surface – avoid chipping
- **High accuracy**: at least +/-1µm
- And **high throughput**

Take advantage of wafer-to-wafer expertise → **And adapt process flow for die-to-wafer**

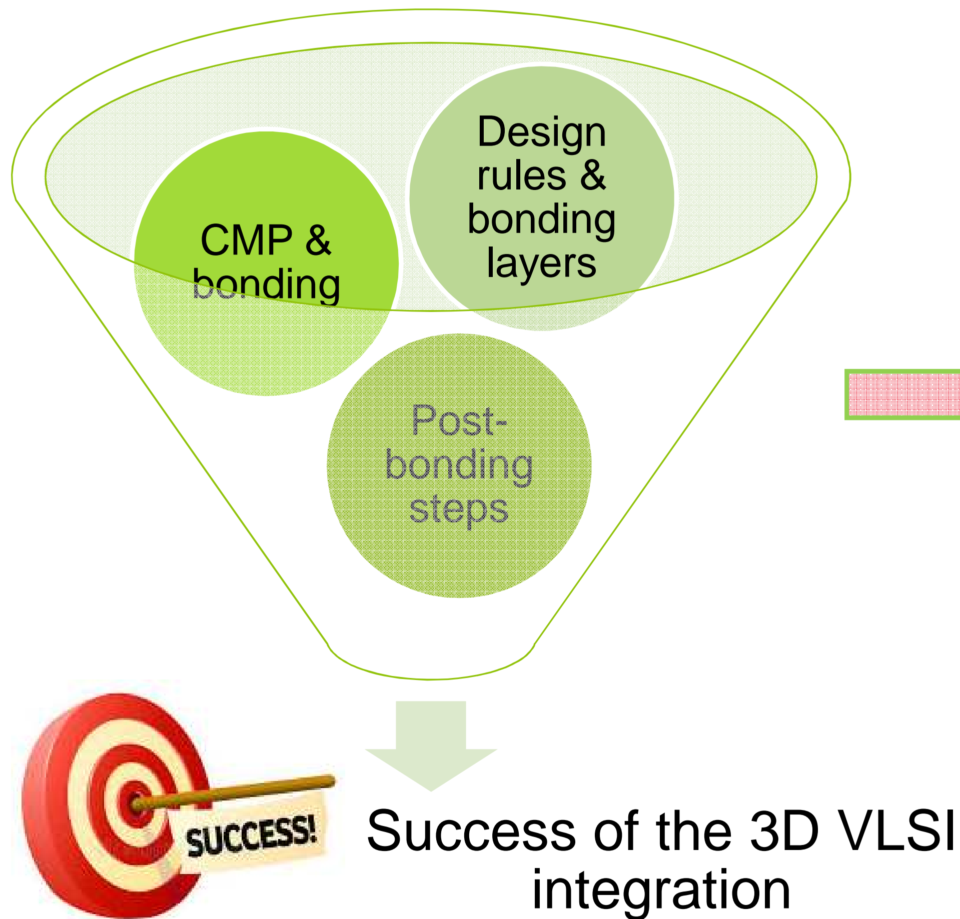
....TO DIE-TO-WAFER HYBRID BONDING FLOW





Take benefit of wafer-to-wafer expertise → **And adapt process flow for die-to-wafer**

3D 300 * @ LETI = A SINGLE SITE FOR THE FULL 3D INTEGRATION

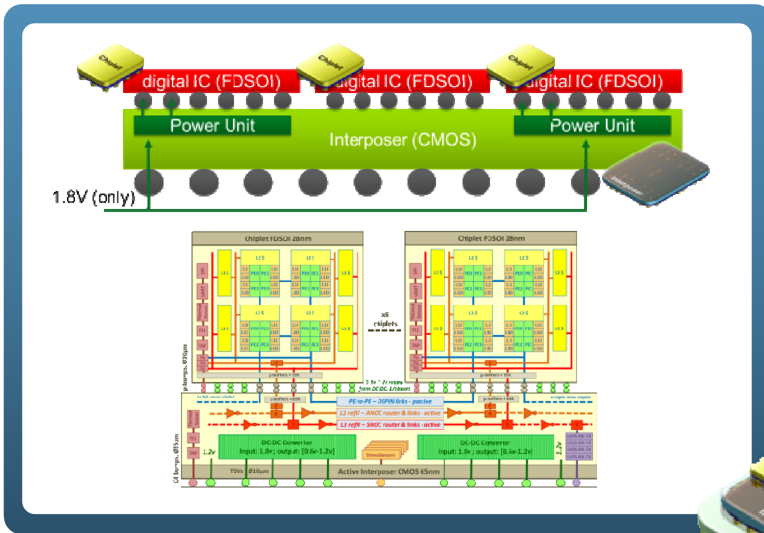


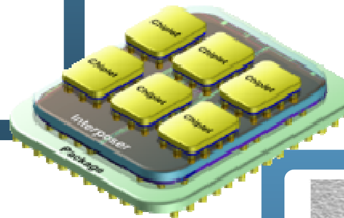
- Design rules provided to the designers by Leti
- Specification of planarization / roughness… for sublevels (and bonding layers) given by Leti
- Bonding layer managed at Leti
- CMP, bonding (WtW, DtW) done at Leti
- Post bonding management: thinning, interdie-filling,TSVs … done at Leti

** Also available in 200mm wafers*

FROM TECHNOLOGY TO TEST CASE (1/2)
3DSOC DEMONSTRATION: INTACT, ACTIVE INTERPOSER

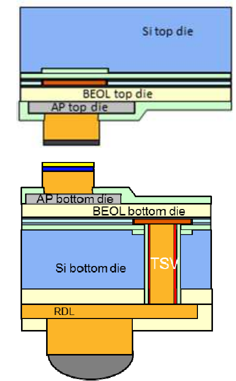
➡ INTACT: Active interposer for many-cores: 96 cores compute fabric



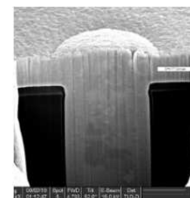


Heterogeneous 3D partitioning for high energy efficiency and reduced cost

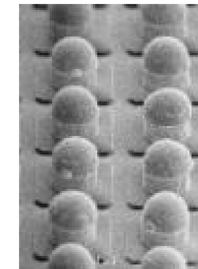
- **28nm FDSOI Chiplets (x6)**
  - Low-power compute fabric
  - Wide voltage range (0.6V – 1.2V)
  - Body biasing for logic boost & leakage ctrl
- **65nm Active Interposer**
  - Power unit (switched cap DC-DC conv.)
  - Interconnect (network-on-chip)
  - Test, clocking, thermal sensors, etc.



- **Performance Targets**
  - **100 GOPS**
  - **10 GOPS/Watt**
  - **25 Watts total**
- **Cache Coherent Compute Fabric**
  - 96 cores (MIPS-32bit)
  - L1/L2/L3 coherent caches
  - Implemented with 3D-plugs
  - Full support of Linux OS



TSV
Ø 10µm
Height 100µm



µ-bumps or Direct Hybrid Bonding
Ø 10 µm
Pitch 20 µm

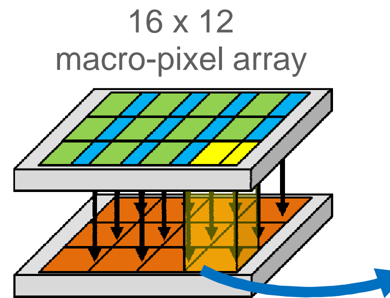
FROM TECHNOLOGY TO TEST CASE (2/2)
SENSOR/LOGIC STACK: RETINE, SMART IMAGER

➡ RETINE: a 3D stacked in-focal-plane vision chip

Our cluster (macro-pixel) approach:
High-interconnection density

- **Top chip: Pixels + ADC Array**
  - In-focal-plane ADC
  - 1024 x 768 BSI pixels
  - Pixel size: 12µmx12µm
- **Bottom chip: Memory + Processing**
  - 3072 processing elements
  - Embedded memory:
    - 98 kB data memory
    - 65+73 kB instruction memory

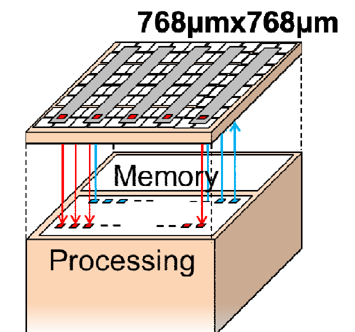
16 x 12
macro-pixel array

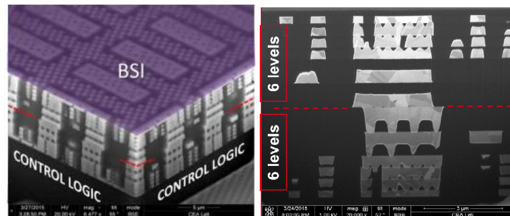


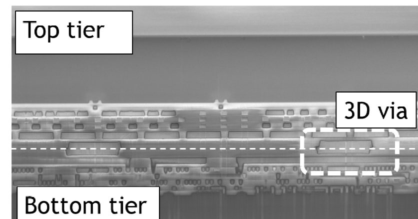
Macro-pixel detail

Top tier
- 16 ADC
- 64 x 64 BSI pixels

Bottom tier
- 16 processing elements
- Local memory







Wafer Level Hybrid Bonding
Pitch 25 µm

- **Performance measured**
  - 5500 frames per seconds
  - 85 GOPS/W
- **Further increase data rate**
- **Reduce processing latency**
- **Large inter-pixel processing capabilities**

L. Millet & Al, 5500fps 85GOPS/W 3D stacked BSI vision chip based on parallel in-focal-plane acquisition and processing, VLSI 2018

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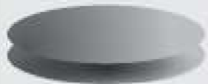
TO CONCLUDE…

3D packaging technologies are key for next CMOS image sensors
…Many other applications will benefit from smartphone early dev

3DVLSI Leti offer: a complete range of technologies including design & simulation

COOLCUBE™

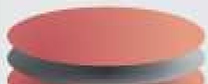


- Demonstration of test vehicles on various CMOS nodes
- Exploration of process integration routes on advanced technology nodes

WAFER TO WAFER

- Demonstration of fine pitch (< 1 µm) hybrid bonding
- Exploration of ultrafine pitch (<500 nm) hybrid bonding

WAFER TO WAFER



- Exploration & demonstration of 3-level-wafer stacking of heterogeneous chips

DIE TO WAFER

- Architecture partitionning of complex computing chips
- Early optimization studies of process flow, test, dicing before bonding….)
- Early stage prototypes and demonstrators
- Option for high-throughput process route using self-assembly

APPLICATIONS

Neuromorphic Accelerators

Implants & Wearables

HPC

Display

Lighting

Imagers

NANOELEC

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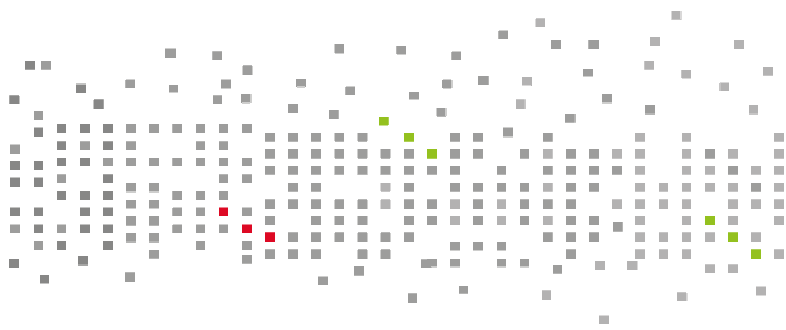

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